

*Amendments to the Claims*

The listing of claims will replace all prior versions, and listings of claims in the application.

1. - 15. (Cancelled)

16. (Currently Amended) A system for packet classification, comprising:

a pre-processor to receive a packet header of an incoming packet, the packet header including a field, and to assign an associated identifier to the field;

a first memory device, the first memory device including a first set of binary patterns;

a second memory device, the second memory device including a second set of binary patterns;

a third memory device, the third memory device including instructions for applying [[one of]] either the first [[and]] set of binary patterns or the second [[sets]] set of binary patterns to the associated identifier assigned to the field of the incoming packet; and

a processor to apply the instructions to the field to match the field to one of the patterns in the first set of binary patterns or second set of binary patterns.

17. (Original) The system of claim 16, wherein the field is a network address.

18.     (Previously Presented)   The system of claim 16, further comprising: a fourth memory device, the fourth memory device including a result corresponding to a matched pattern received from the processor.

19.     (Previously Presented)   The system of claim 16, further comprising: means for determining priority among one or more matched patterns.

20.     (Original)   A method for packet classification, comprising:  
receiving a packet header of an incoming packet, the packet header including a field;  
assigning an associated identifier to the field;  
maintaining a first set of binary patterns and a second set binary patterns;  
applying one of the first and second sets of binary patterns to the associated identifier assigned to the field of the incoming packet; and  
matching the field of the incoming packet to one of the patterns in the first set of binary patterns or second set of binary patterns.

21.     (Original)   An apparatus for packet classification, comprising:  
(a) a processor array containing a plurality of processing elements, wherein each processing element is configured to: (i) compare a classification record derived from an incoming packet with one or more patterns associated with rules to be enforced by performing programmed relational operations, and (ii) capture state information in a shift register that is shared by more than one of the processing elements;

(b) an instruction decoder to suspend operations for a set of the processing elements and to restart operations for the set of processing elements;

(c) at least one priority encoder to determine a highest priority from the state information from the shift registers; and

(d) a record memory that is addressed for read and write capabilities, wherein writes are executed to indicate which of several simultaneously processed packets is being submitted to the apparatus for packet classification, and wherein reads are executed to indicate which bit or bits are to be provided to the processor array from all of the simultaneously processed packets.

22.     (Original)   The apparatus of claim 21, wherein the programmed relational operations include equality, less than or equal to, and greater than or equal to operations.

23.     (Original)   The apparatus of claim 21, further comprising an instruction memory containing instructions to: (i) select which bit or bits of the simultaneously processed packets are to be examined by the processor array, and (ii) determine how the selected bit or bits are to be compared against one or more of the patterns.

24.     (Original)   The apparatus of claim 23, wherein the instructions in the instruction memory are a classification program, wherein the classification program contains further instructions to divide the classification program into subsets of sequential instructions, each of which represents a subset of the rules defined by the classification program.

25. (Original) The apparatus of claim 24, wherein a prioritized relationship exists between a pair of the subsets of the rules.

26. (Original) The apparatus of claim 24, wherein the record memory is rewritable during execution of the classification program such that a result from the priority encoder can be subsequently examined by the classification program.

27. (Original) The apparatus of claim 26, wherein the result includes the current highest priority match as determined by the priority encoder.

28. (Original) The apparatus of claim 24, wherein one or more bits selected from one of the classification records in the record memory can determine a subset of instructions in the classification program to apply to one or more of the classification records.

29. (Original) The apparatus of claim 28, wherein the one or more bits selected are selected under programmed control.

30. (Original) The apparatus of claim 28, wherein the classification program can be seamlessly updated.

31.     (Original)   The apparatus of claim 28, wherein the effective size of the classification program can be increased.

32.     (Original)   The apparatus of claim 28, wherein the number of processing elements applied to a single incoming packet can be scaled.

33.     (Original)   The apparatus of claim 28, wherein the number of simultaneously processed packets can be scaled.

34.     (Original)   The apparatus of claim 28, wherein the number of packet bits used to select a classification program can be scaled.

35.     (Original)   The apparatus of claim 28, wherein multiple instances of the apparatus are cascaded such that a first instance of the apparatus feeds into a second instance of the apparatus.

36.     (Original)   The apparatus of claim 21, wherein multiple instances of the apparatus are cascaded such that a first instance of the apparatus feeds into a second instance of the apparatus.